Session 16 Overview

Power Distribution and Management

Chair: Alice Wang, *Texas Instruments, Dallas, Texas*

Associate Chair: Jos Huisken, *Silicon Hive, Eindhoven, The Netherlands*

There is an extreme range of power constraints in today's electronic applications, ranging from high-performance servers to low-power personal-health-care products. Traditionally, chips in these domains have been designed with a fixed power-supply-voltage and frequency. With the explosion in variability in today's nanoscale circuits, fixed operating points with large process variations require wide design margins, incurring a cost in power consumption or performance. Squeezing the most out of these designs involves optimizing the power distribution and management methods. To do this, two independent technologies are needed: the ability to measure accurately the chip behavior and the ability to use this information to control system parameters such as frequency and voltage.

The seven papers in the session present techniques allowing designers to take advantage of adaptive systems to reduce design margins and either improve performance or reduce power dissipation. For the coming years, this kind of adaptive control will be essential for maintaining growth in performance and improving battery life in the face of increasingly unpredictable circuits and environments.

Paper 16.1 from Intel and HaoKai describes an active on-die damping circuit to suppress resonance in the power distribution between the die and the power delivery network. Reducing peak-to-peak noise allows for increased operating frequency, robustness against hold time failures and improved chip lifetimes by reducing gate oxide stress.

The next two papers highlight on-die supply-noise sensors to provide valuable insight into supply-noise characteristics for diagnosis and for real-time operation. Paper 16.2 from Kobe U and Renesas employs two different types of sensors. Built-in probing circuits that measure power and ground voltages at 120 fine-grain locations across a device, as well as higher accuracy sampling monitor circuits measuring at a higher precision at 26 locations. Paper 16.3 from Fujitsu and A-R-Tec performs real-time monitoring by using histograms and counters to focus on the worst noise events while the chip is in normal operation.

Adaptive voltage supply and body-bias techniques are used to optimize power-performance trade-offs and lifetime effects. Paper 16.4 from Intel, Tyfone and Oregon State U selectively maximizes average performance or improves energy-efficiency by adapting frequency, supply voltage and body bias to react to changes in supply noise, temperature and transistor aging. Paper 16.5 from National Chung Cheng U highlights an ultra-low-power RISC core using aggressive voltage and body-bias scaling to run down to an astonishingly low 230mV, while significantly improving operating speeds. Paper 16.6 from Hitachi and Renesas describes an active resource manager controlling the core frequencies and data bandwidth while monitoring on-die thermal changes.

Paper 16.7 from IBM gives for the first time, cycle-by-cycle supply noise traces of split- and connected-core power supplies with various combinations of active and inactive cores. These results give designers insight into noise interaction between cores and enable power grid optimizations for the class of increasingly heterogeneous chips with multiple power domains.

16.1 On-Die Supply-Resonance Suppression Using Band-Limited Active Damping **1:30 PM**

J. Xu, Intel, Hillsboro, OR

The impedance of a microprocessor power-delivery network peaks at ~140MHz, resulting in power-grid resonance, which lowers operating frequency and compromises reliability. A suppression circuit uses an active-damping technique with a maximum of 12.7dB peak-to-peak noise reduction from 70 to 250MHz in a 90nm CMOS process.

16.2 Fine-Grained In-Circuit Continuous-Time Probing Technique of Dynamic Supply Variations in SoCs **2:00 PM**

M. Fukazawa, Kobe University, Kobe, Japan

Fine-grained built-in probing circuits are distributed at 120 locations on the SoC to allow continuous-time monitoring of power-supply variations. On-die high-precision sampling circuits with 800μV/100ps resolution allow probing of 26 chip-wide locations of the CPU core including SRAM modules. Analog waveforms and peak-voltage measurements show confirmation of dynamic operation-mode transitions.

16.3 On-Die Supply-Voltage Noise Sensor with Real-Time Sampling Mode for Low-Power Processor Applications **2:30 PM**

T. Sato, Fujitsu Laboratories, Kawasaki, Japan

A real-time on-die noise sensor continuously detects up to 100 noise events per second without disturbing processor operations, using a 400kb/s serial interface. The noise sensor uses histogram counters and variable detection windows. The sensor measures periodic and single-events in real time. The noise sensor is implemented in a 90nm CMOS testchip.

16.4 Adaptive Frequency and Biasing Techniques for Tolerance to Dynamic Temperature-Voltage Variations and Aging

J. Tschanz, Intel, Hillsboro, OR **3:15 PM**

Temperature, voltage, and current sensors monitor the operation of a TCP/IP offload accelerator engine fabricated in 90nm CMOS, and a control unit dynamically changes frequency, voltage, and body bias for optimum performance and energy efficiency. Fast response to droops and temperature changes is enabled by a multi-PLL clocking unit and on-chip body bias. Adaptive techniques are also used to compensate performance degradation due to device aging, reducing the aging guardband.

16.5 A 230-to-500mV 375kHz-to-16MHz 32b RISC Core in 0.18μm CMOS **3:45 PM**

J-S. Chen, National Chung-Cheng University, Chia-Yi, Taiwan

An ultra-low voltage 32b RISC core is realized with an ultra-low-voltage CMOS technique. An operating frequency of 16MHz is attained with a supply voltage of 500mV and a frequency of 375kHz is attained with a supply voltage of 230mV. Compared to the state-of-the-art-operating from 250 to 500mV, this work offers 6.7× and 125× respective improvements in operating speed.

16.6 Embedded SoC Resource Manager to Control Temperature and Data Bandwidth **4:15 PM**

M. Saen, Hitachi, Tokyo, Japan

A 0.4mm^2 SoC resource manager controls operating frequency and allocates data bandwidth using various monitored information such as temperature, frequency of IP blocks and number of operations executed. Results show an increase of allowable temperature range by 30°C for real-time operations of two processor cores and two media processing cores. The design is fabricated in an 8M 90nm CMOS process.

16.7 Comparison of Split- Versus Connected-Core Supplies in the POWER6™ Microprocessor **4:45 PM**

N. James, IBM, Austin, TX

The POWER6™ is a dual-core microprocessor fabricated in a 65nm SOI process with 10 levels of low-k copper interconnects. Chips with split- and connected-core power supplies are fabricated, modeled, and tested, showing both the advantages and disadvantages of each. On-chip noise measurements are compared to simulation. The noise measurements and simulation both show that the shorted core power grid design has less noise and a higher maximum frequency.